

ABSTRACT

A design and method of fabrication for a semiconductor package is described. A solder bumped semiconductor chip is assembled to a metallized package substrate utilizing the solder bumps. The interconnecting solder bumps are properly constrained at assembly by the introduction of a no-flow underfill between the chip and the substrate. The no-flow underfill constrains the solder of the solder bumps so as to maintain the desired size and shape.